

Appl. No. 10/708,108
Amdt. dated November 5, 2004
Reply to Office action of October 8, 2004

AMENDMENTS TO THE CLAIMS

5 Claim 1 (currently amended): A mixed-mode process for integration circuits comprising:

providing a semiconductor substrate, a surface of the semiconductor substrate comprising at least a first conductor formed in a first conductive region, at least a second conductor formed in a second conductive region, at least a
10 metal-oxide-semiconductor (MOS) transistor formed in a MOS transistor region, and at least a capacitor formed in a capacitor region;

forming a mask on the semiconductor substrate to cover the MOS transistor, the first conductor, and the capacitor and to expose the second conductor;

performing a first etching process to remove a specific thickness of the second
15 conductor; and

performing a first ion implantation process to dope the second conductor with first type dopants;

wherein the order of the first etching process and the first ion implantation process can be switched.

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Claim 2 (original): The mixed-mode process of claim 1 further comprising the following steps for forming the first conductor, the second conductor, the MOS transistor, and the capacitor:

sequentially forming a gate oxide layer and a first polysilicon layer on the
25 semiconductor substrate;

performing a first photo-etching-process (PEP) to remove portions of the first polysilicon layer to simultaneously form a gate structure and a bottom electrode plate structure of the capacitor respectively in the MOS transistor region and the capacitor region;

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sequentially forming an inter polysilicon oxide (IPO) layer and a second polysilicon layer doped with second type dopants on the semiconductor substrate to cover the gate structure and the bottom electrode plate structure;

- 5 performing a second PEP to remove portions of the second polysilicon layer to form the first conductor, the second conductor, and a top electrode plate of the capacitor, respectively, in the first conductive region, the second conductive region, and the capacitor region;

- 10 forming a dielectric layer on the semiconductor substrate to cover the first conductor, the second conductor, the gate structure, and the capacitor; and

performing a second etching process to remove portions of the dielectric layer to form a spacer on either sides of the first conductor, the second conductor, the capacitor, and the gate structure.

- 15 Claim 3 (original): The mixed-mode process of claim 2 wherein the first polysilicon layer is a doped polysilicon layer or an undoped polysilicon layer followed by an ion implantation process.

- 20 Claim 4 (original): The mixed-mode process of claim 2 wherein a polycide layer is formed before performing the first PEP process, and portions of the polycide layer is removed by the first PEP process.

- 25 Claim 5 (original): The mixed-mode process of claim 4 wherein portions of the first polysilicon layer and the polycide layer in the gate structure is employed as a gate of the MOS transistor of the integration circuits.

Claim 6 (original): The mixed-mode process of claim 4 wherein portions of the first polysilicon layer and the polycide layer in the bottom electrode plate structure is employed as a bottom electrode plate of the capacitor.

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Claim 7 (original): The mixed-mode process of claim 4 wherein the polycide layer comprises tungsten silicide.

- 5 Claim 8 (original): The mixed-mode process of claim 2 wherein the first type dopants are N-type dopants and the second type dopants are P-type dopants.

Claim 9 (original): The mixed-mode process of claim 2 wherein the first dopants are P-type dopants and the second type dopants are N-type dopants.

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Claim 10 (original): The mixed-mode process of claim 2 wherein the second PEP utilizes the IPO layer as a stop layer.

- 15 Claim 11 (original): The mixed-mode process of claim 2 wherein a wet dip process is performed after the second PEP to remove portions of the IPO layer and to preserve the IPO layer between the bottom electrode plate structure and the top electrode plate employed as a capacitor dielectric layer of the capacitor.

- 20 Claim 12 (original): The mixed-mode process of claim 2 wherein the dielectric layer comprises tetra-ethyloxysilane (TEOS).

- 25 Claim 13 (original): The mixed-mode process of claim 2 wherein either portions of the surface of the semiconductor substrate within the first conductive region, the second conductive region, or the capacitor region comprise a field oxide layer, and surfaces of the field oxide layer and the gate oxide layer are employed as a stop layer for the second etching process used for the formation of the spacers.

Claim 14 (original): The mixed-mode process of claim 1 wherein the conductors in the first conductive region and the second conductive region are employed as resistors

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of the integration circuits, and the mask is a high resistance (HR) mask.

5 Claim 15 (original): The mixed-mode process of claim 1 wherein the method for
controlling the end of the first etching process comprises using a time mode or an
endpoint mode.

10 Claim 16 (original): The mixed-mode process of claim 1 wherein a second ion
implantation process is performed to form a source and a drain of the MOS transistor
in portions of the semiconductor substrate adjacent to either sides of the gate
structure.

Claims 17-32 (cancelled)